









12. (Original) The circuit of Claim 10, wherein the holding switch circuit further includes a second dummy circuit.
13. (Original) The circuit of Claim 12, wherein the first dummy circuit includes a first n-type transistor including a drain that is coupled to a source of the first n-type transistor, the second dummy circuit includes a second n-type transistor including a drain that is coupled to a source of the second n-type transistor, and wherein the first boosted switch circuit includes a third n-type transistor.
14. (Original) The circuit of Claim 12, wherein the first dummy circuit is configured to receive an inverted boosted signal, the second dummy circuit is configured to receive another inverted boosted signal, and wherein the inverted boosted signal and the other inverted boosted signal are each a substantial inverse of the boosted signal.
15. (Original) The circuit of Claim 12, wherein the first and second dummy circuits each include an associated width that is approximately half of a width that is associated with the first boosted switch circuit.
16. (Original) The circuit of Claim 12, wherein the first dummy circuit is coupled between the second node and the first boosted switch circuit, and wherein the second dummy circuit is coupled between the first boosted switch circuit and the third node.
17. (Original) The circuit of Claim 12, wherein the holding switch circuit further includes:  
a second boosted switch circuit that is configured to open and close in response to another boosted signal, wherein the other boosted signal is substantially the same as the boosted signal.



operable to provide the digital output signal at a first time and a second processing channel that is operable to provide the digital output signal at a second time; and

a sample-and-hold circuit that is interleaved by at least two such that a speed of the sample-and-hold circuit is approximately at least doubled without substantially decreasing the processing time allowed for the processing circuit.

22. (New) A circuit for sampling and holding, comprising:

a processing circuit that is interleaved such that the processing circuit includes a first processing channel and a second processing channel;

a first sample-and-hold channel that is coupled to the first processing channel;

a boost circuit that is coupled to the first sample-and-hold channel, wherein the boost circuit is capable of providing a boosted voltage that exceeds a power supply voltage; and

a second sample-and-hold channel that is coupled to the second processing channel.